14 - MOSFETs Other Apps Name:___________________________

Only a few problems for review, with solutions provided. The extra time today can be used for old test review!

This first problem tests your ability to learn and interpret contemporary knowledge about the state of the art in your field of study. Check out this article: http://spectrum.ieee.org/semiconductors/devices/transistors-could-stop-shrinking-in-2021

(a) What is the smallest physical gate length that is now being projected and when? *Answer: ~ 10 nm. ~2021*

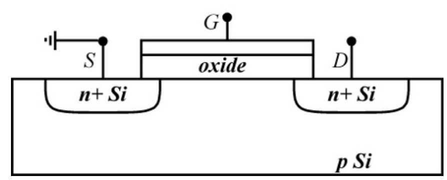
(b) Why are companies going to stop so much focus on making gate lengths smaller? *Answer: the current thinking is that to keep doubling the number of transistors every two years (Moore's law) that companies are going to instead focus on less challenging approach of 3D architectures. Although 'less challenging' this will still be incredibly difficult.*

(c) See the figure 'New Geometry'. Explain or diagram how FinFETs, Lateral Nanowires, and Vertical Nanowires all work (do you best to figure it out, hint, it is always about using a gate voltage for depleting or enhancing a Silicon connection between a source and a drain).

Consider an <u>ideal</u> n-channel MOSFET on a p-Si substrate with the following characteristics (you may or may not need all the information provided below):

$N_a = 10^{16}/cm^3$
Oxide thickness = 50 nm
Area of gate = 1x1 μm

$\varepsilon_{Si}\varepsilon_0 = 11.8 \times 8.854\times10^{-14}$ F/cm = 1.0×10^{-12} F/cm
$\varepsilon_{oxide}\varepsilon_0 = 4 \times 8.854\times10^{-14}$ F/cm = 3.4×10^{-13} F/cm
$\phi_F = 0.347$ eV



(a) Calculate the threshold voltage for this device.

(b) You decide to make a new device with a thinner oxide and therefore a lower threshold voltage, how much thinner should the oxide be if the threshold voltage is to be lowered by 0.5V?

$$W_m = 2\sqrt{\frac{\epsilon_s \cdot \Phi_F}{q \cdot N_a}} = 2\left[\frac{11.8 \cdot 8.85 \cdot 10^{-14}\,\frac{F}{cm} \cdot 0.347V}{1.6 \cdot 10^{-19} C \cdot 10^{16}\,\frac{1}{cm^3}}\right]^{1/2} = 3.01 \cdot 10^{-5}\,cm = 0.301\,\mu m$$

a) $W_m = 300\text{ nm}$ (given) ∴ $Q_d = -qN_a W_m = -47\text{ nC/cm}^2$

$V_t = -\frac{Q_d}{C_i} + 2\phi_F$, need $C_i = \frac{\varepsilon}{d} = \frac{3.4\times10^{-13}\text{ F/cm}}{50\times10^{-7}\text{ cm}} = 68\text{ nF/cm}^2$

∴ $V_t = \frac{47\text{ nC/cm}^2}{68\text{ nF/cm}^2} + 2\times0.347\text{V} = 0.691 + 0.694 = 1.385\text{ V}$

b) lower V_t by 0.5V? ∴ $V_i = 0.191\text{ V}$ $(0.691 - 0.5\text{ V})$

∴ $C_i = -Q_d/V_i = \frac{47\text{ nC/cm}^2}{0.191\text{ V}} = 240\text{ nF/cm}^2$

$C_1 d_1 = C_2 d_2 \rightarrow d_2 = d_1 \frac{C_1}{C_2}$

or $d = 50\text{ nm}\cdot\frac{68\text{ nF/cm}^2}{240\text{ nF/cm}^2} = 14\text{ nm}$

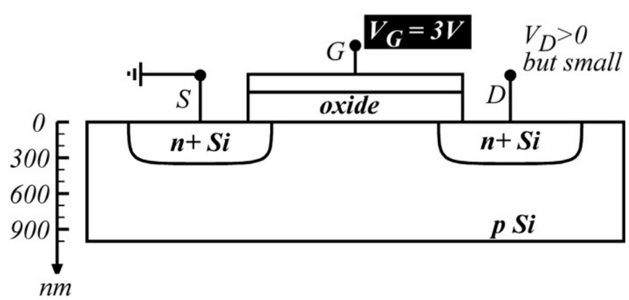
$C = \frac{\varepsilon A}{d}$

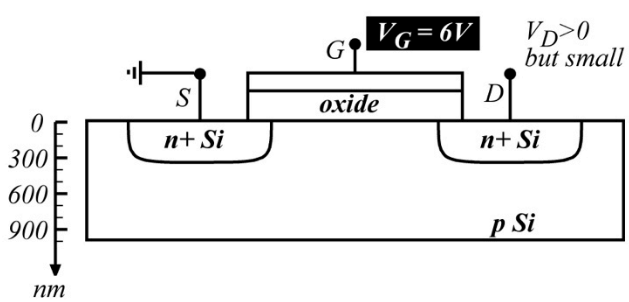
or

$C\,d = \varepsilon A = \text{constant}$

The following is for an ideal (flat band at V_G=0) enhancement-mode n-channel MOSFET (NMOS) with a threshold voltage of V_T =3V and a value for W_m of 300 nm. QUALITATIVE ANSWERS / NO EQUATIONS CALCULATIONS ARE NEEDED.

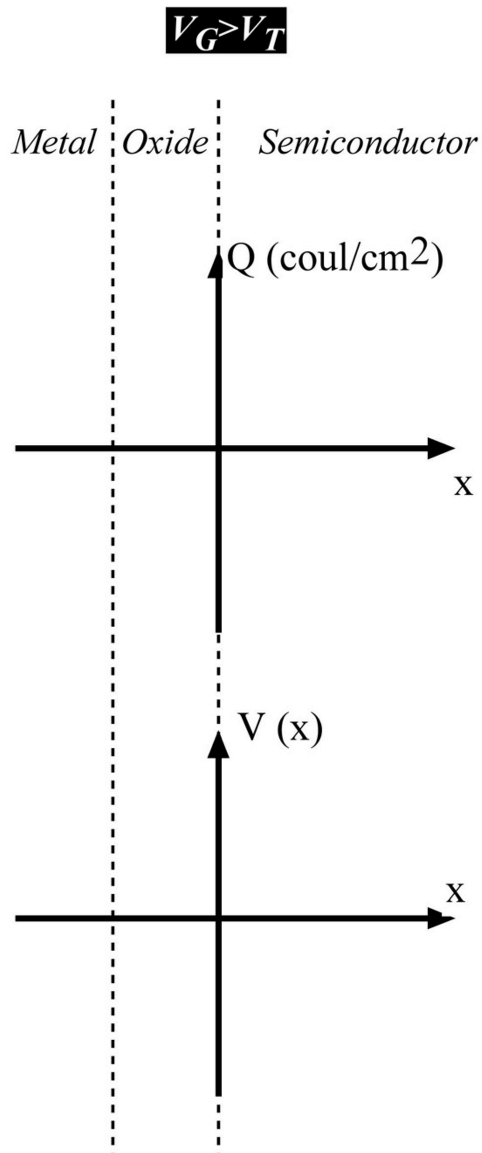
(a) We bias the MOSFET as labeled below. Label on the diagrams the depletion width into the p-type semiconductor.

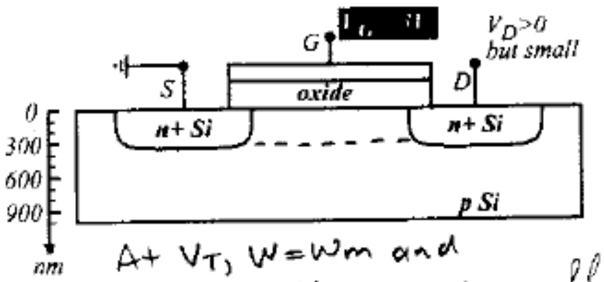




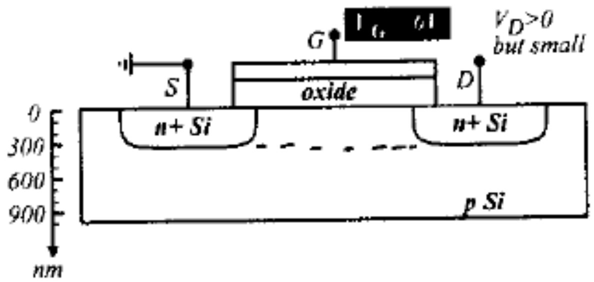
(c) Plot voltage Q(x) and V(x) vs. distance x for the MOS portion of an n-channel MOSFET for the case of $V_G>V_T$. On the plots, properly label all charges, voltages, and also the location of W_m (the end of the depletion region in the semiconductor).

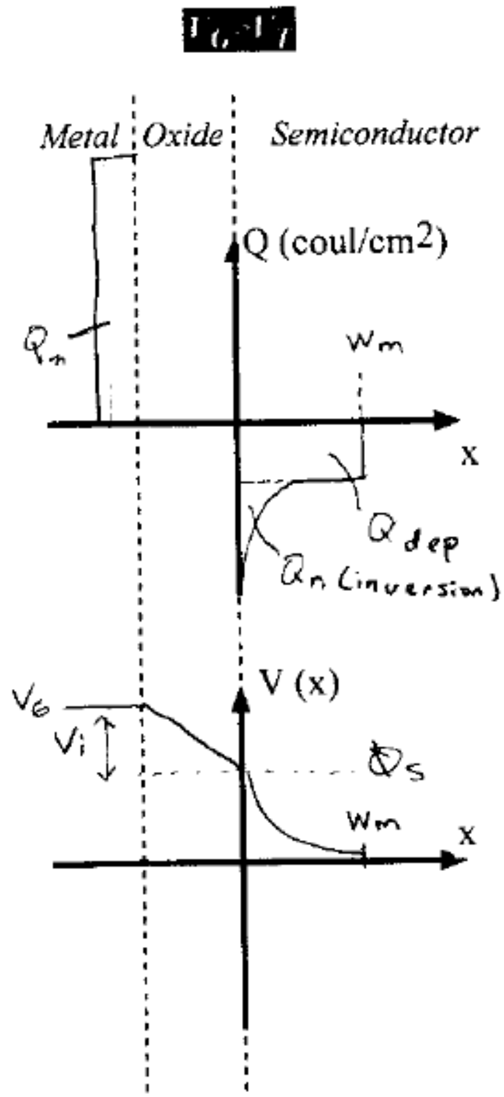
(b) [5 pts] How would we change the semiconductor materials in the device above to make it a p-channel MOSFET (PMOS).





At V_T, $W=W_m$ and W_m is the maximum!!





b) [3 pts.] How would we change the semiconductor materials in the device above to make it a p-channel MOSFET (PMOS).

Substrate ⇒ n Si

Source and Drain ⇒ p+ Si